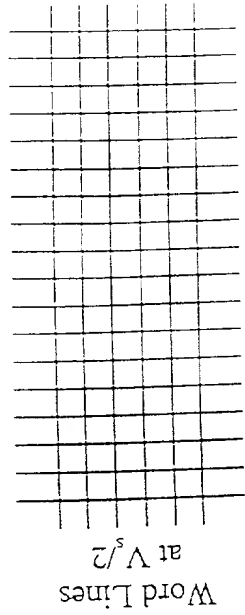


FIG.2

3 Level Passive Matrix Switching Protocol

- t_0 : word line latched, active pulldown to 0
- t_1 : bit line clamp released - sense amp on
- t_2 : bit line decision - data latched
- t_3 : word line returned to quiescent $V_s/2$
- t_4 : write data latched on bit lines
- t_5 : word line pulled to V_s - set/reset caps
- t_6 : word line returned to quiescent $V_s/2$
- t_7 : bit lines actively returned to V_s clamp
- t_8 : read/write cycle complete

Maximum depolarizing voltage $V_s/2$



Sense Amps biased near V_s

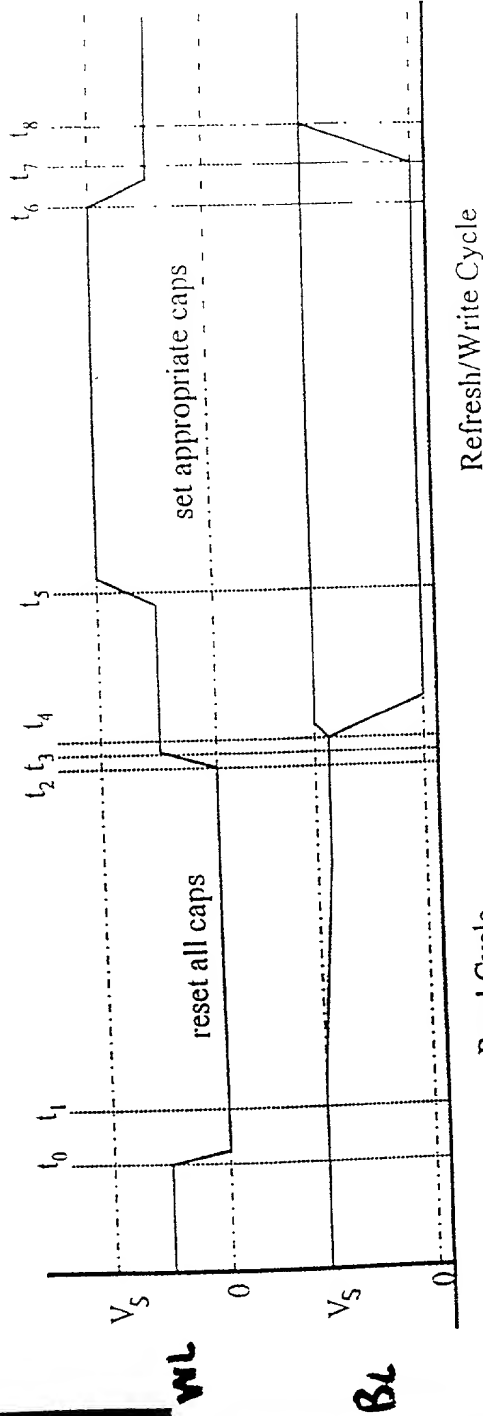


Fig. 4

3 Level Passive Matrix Switching Protocol

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- t_0 : word line latched, active pull μp to V_s
- t_1 : bit line clamp released - sense amp on
- t_2 : bit line decision - data latched
- t_3 : word line returned to quiescent $V_s/2$
- t_4 : write data latched on bit lines
- t_5 : word line pulled to $\mathbf{0}$ - set/reset caps
- t_6 : word line returned to quiescent $V_s/2$
- t_7 : bit lines actively returned to $\mathbf{0}$ clamp
- t_8 : read/write cycle complete

Maximum depolarizing voltage $V_s/2$

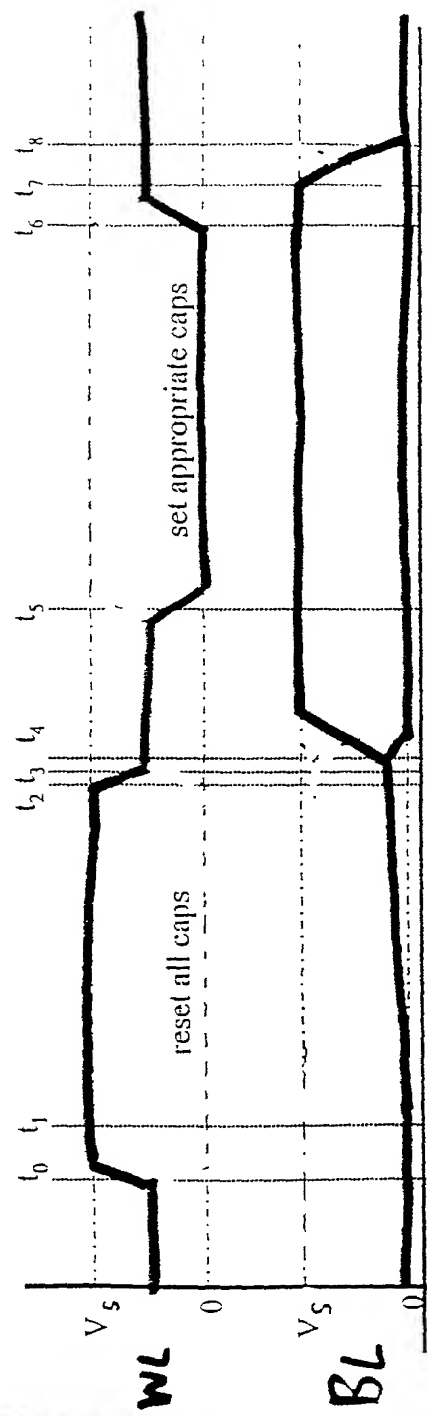
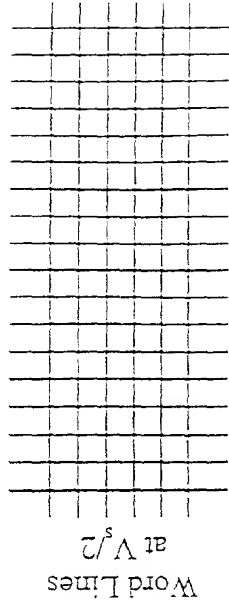


FIG. 5

Refresh/Write Cycle

Read Cycle

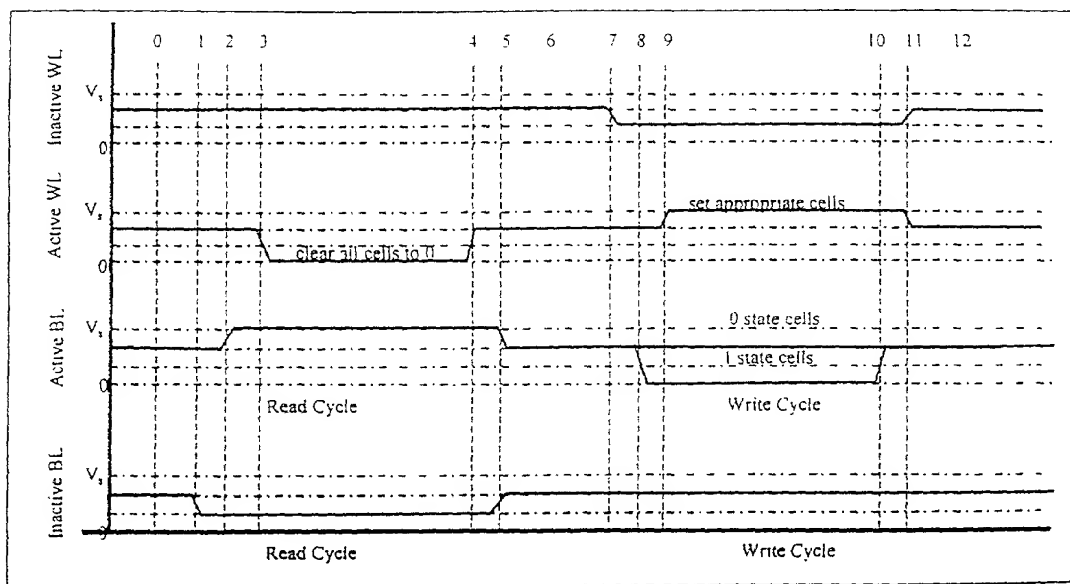


FIG. 6.

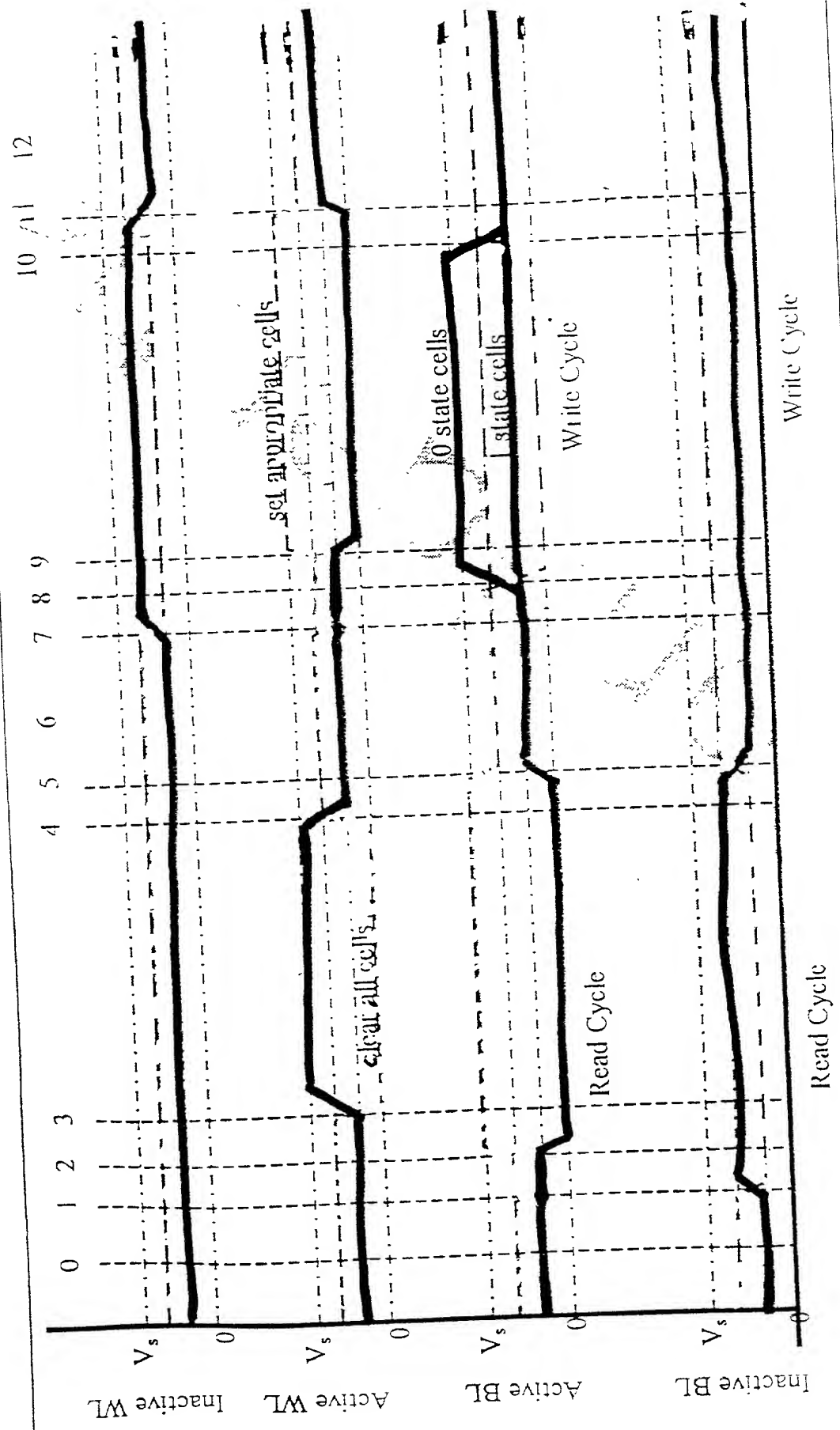


FIG. 7

Five Level Timing Diagram

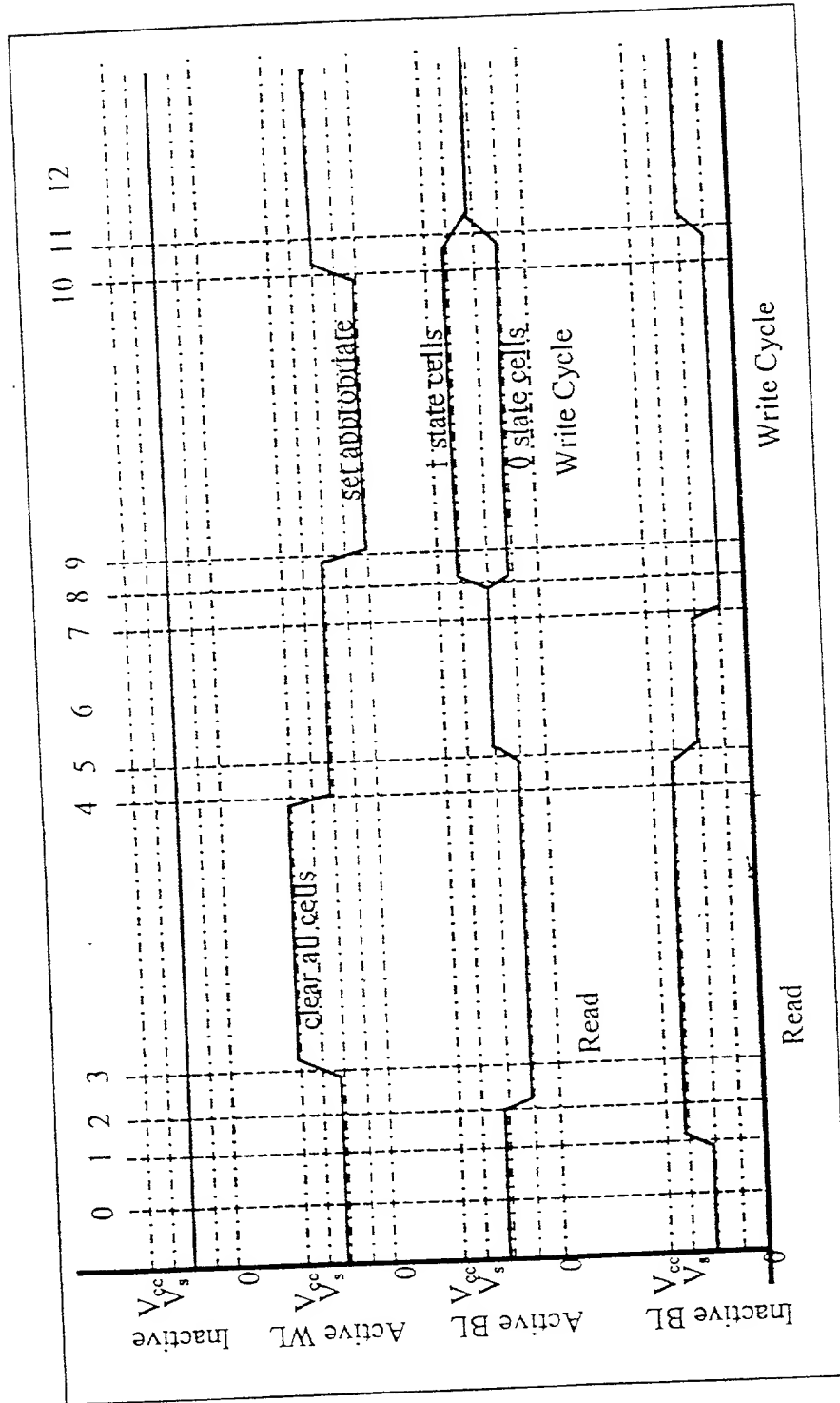


FIG. 9

102201 800000000

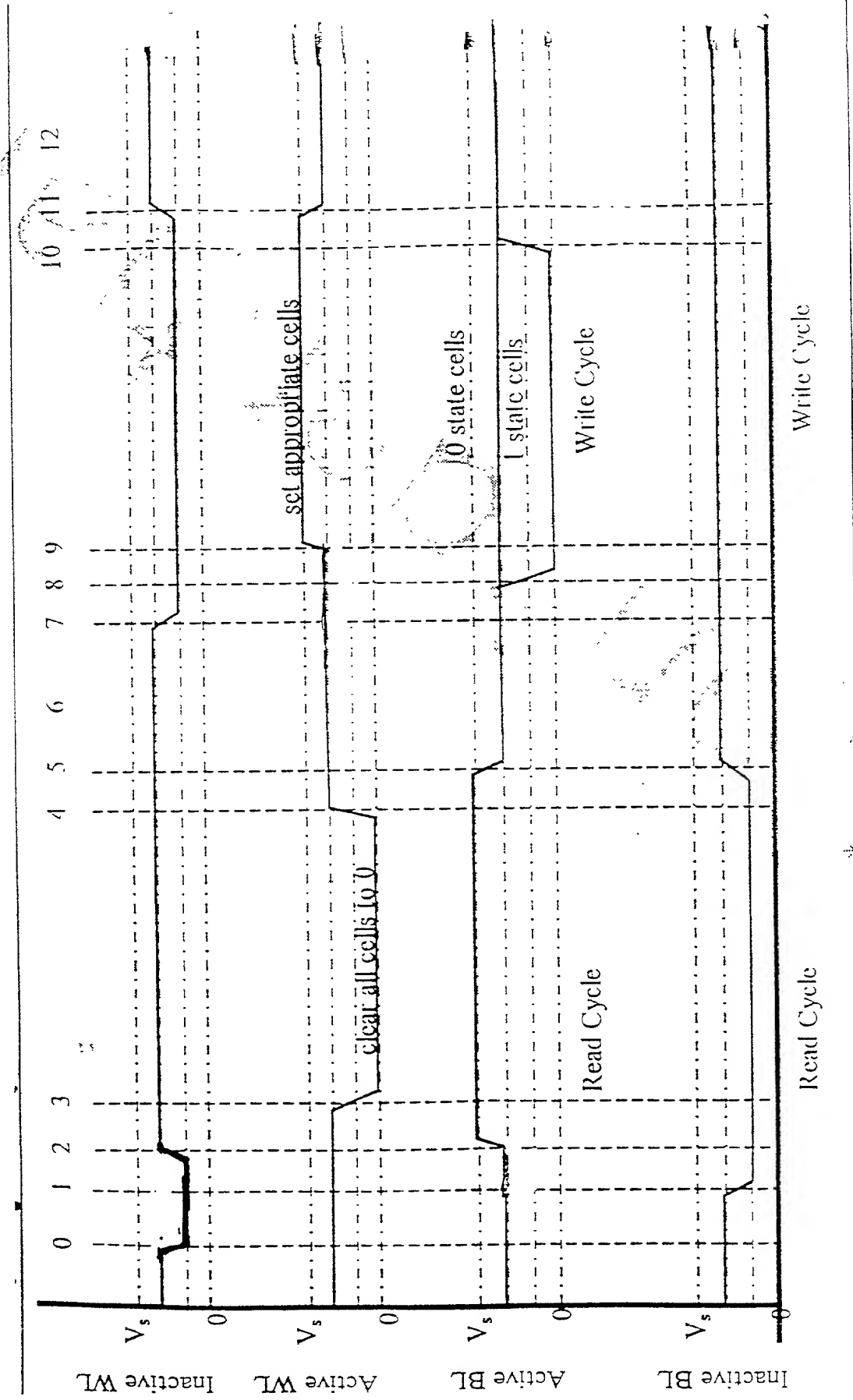


Fig. 10

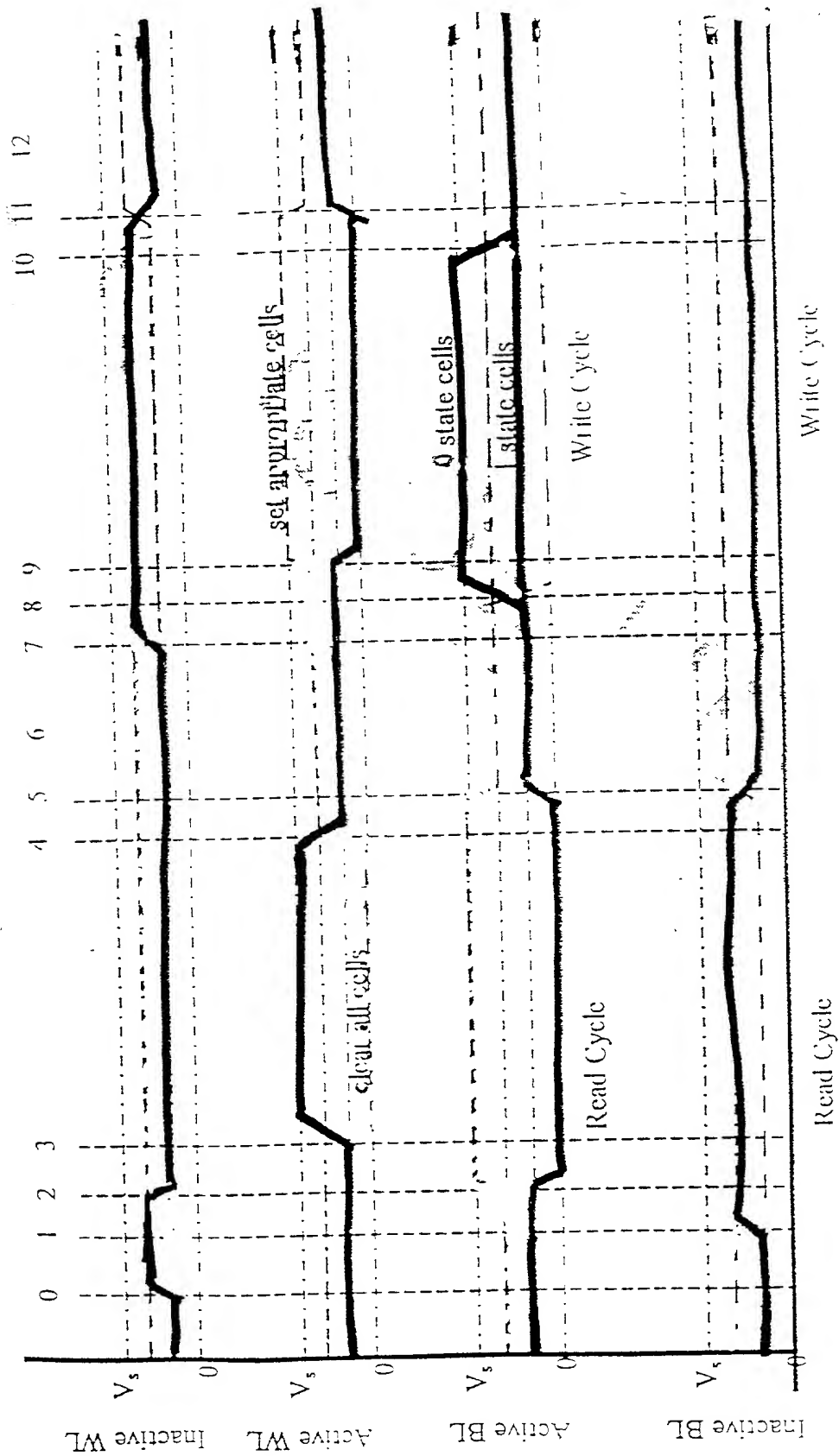


Fig. 11

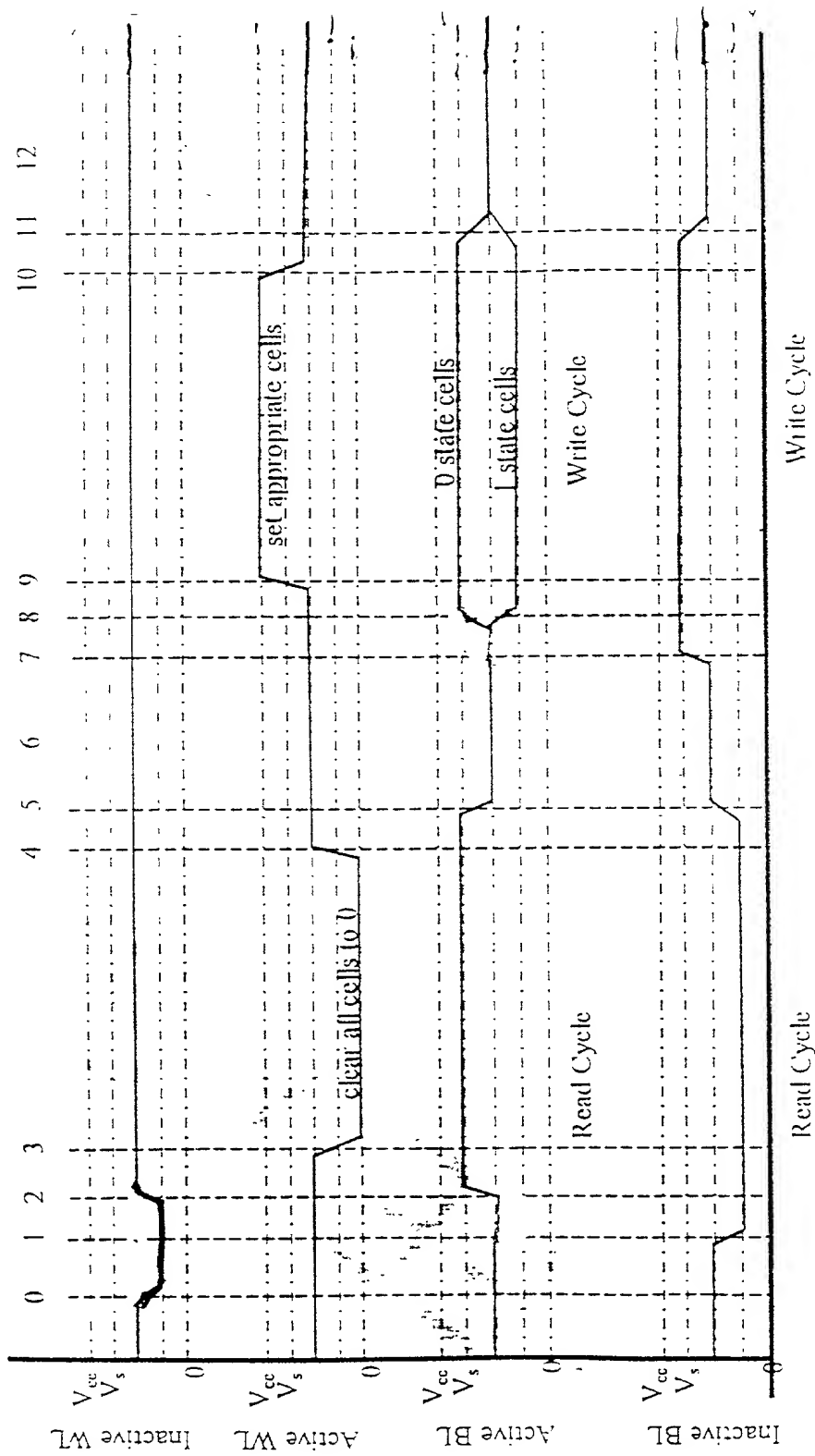


FIG.12

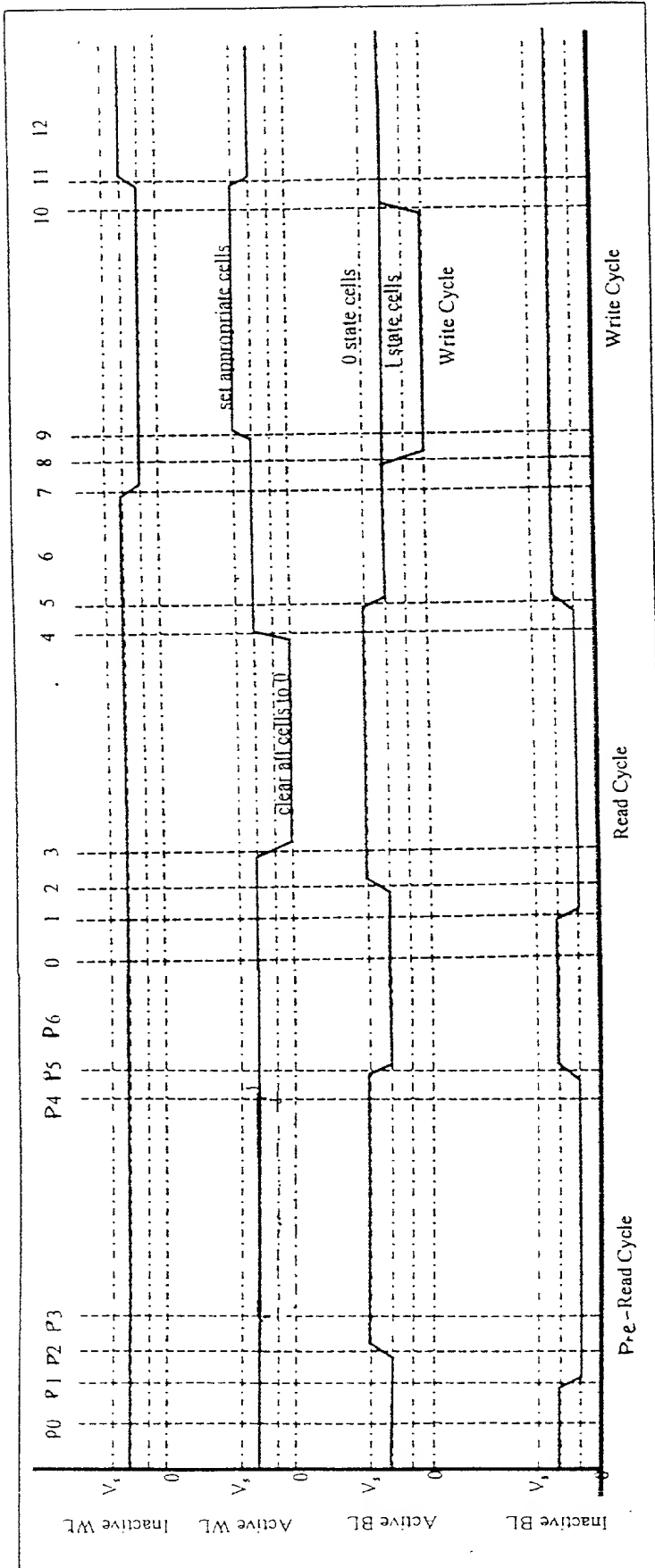


FIG. 14
EXAMPLE OF READ AND WRITE PROTOCOL INVOLVING A PRE-READ REFERENCE CYCLE.

The diagram illustrates a 1T1C array architecture. It consists of a grid of memory cells. The columns are labeled WL1, WL2, WL3, and ACTIVE WL. The rows are labeled SENSE AMPLIFIERS. The ACTIVE WL row is highlighted with a thick black line. The SENSE AMPLIFIERS are represented by black triangles pointing right.

FIG.15

BL 1 BL 2 BL 3